



5-6-05

IFW

[2885/77]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Martin VORBACH et al.
Serial No. : 10/764,159
Filing Date : January 23, 2004
For : METHOD OF HIERARCHICAL CACHING OF
CONFIGURATION DATA HAVING DATAFLOW
PROCESSORS AND MODULES HAVING TWO- OR
MULTIDIMENSIONAL PROGRAMMABLE CELL
STRUCTURE (FPGAs, DPGAs, etc.)

Group Art Unit : 2186
Examiner : Stephen C. Elmore
Confirmation No. : 8160

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION TO CORRECT FILING DATE
and
DATE-IN DISCREPANCY UNDER 37 C.F.R. §1.10(c)

SIR:

Pursuant to 37 C.F.R. §1.10(c), Applicants hereby petition to correct the filing date for the above-identified patent application from "January 24, 2004" to —**January 23, 2004**—.

The instant application was deposited with the United States Postal Service using "Express Mail Post Office to Addressee" service on January 23, 2004. In preparing the application for filing, Applicants affixed the express mail label number, **EV 332 524 594 US**, to the following Application papers: (1) the Transmittal, (2) the first page of the Specification, (3) the Information Disclosure Statement, (4) the Preliminary Amendment, (5) the Drawings, (6) and the Return Receipt Postcard.

On May 3, 2005, while preparing a response to an outstanding Office Action, Applicants noticed that the filing date on the Office Action did not match our internal data sheet, and on further review of the file, Applicants found that the Return Receipt Postcard was incorrectly stamped with a January 24, 2004 date, and that the Filing Receipt and subsequent correspondence from the Patent Office repeated the error.

Applicants looked up the original Express Mail Label receipt (US 332 524 594 US) and confirmed that the "date in" date accorded the application by the U.S. Post Office was indeed the correct date of deposit, —January 23, 2004—. Applicants believe that the error occurred at the Patent Office when the application was incorrectly assigned the date of receipt by the USPTO as the date of filing instead of the date of deposit under 37 C.F.R. §1.10.

Applicants enclose the following documents for consideration in this Petition: (1) the Transmittal, (2) the first page of the Specification, (3) the Information Disclosure Statement, (4) the Preliminary Amendment, which all indicate that Applicants properly labeled each document filed with the application was associated with the Express Mail Label EV 332 524 594 US, and a true copy of the **Express Mail Label EV 332 524 594 US** as signed and stamped by the U.S. Postal Service at 8:23 p.m. on January 23, 2004.

Accordingly, since Applicants did deposit the application properly under 37 C.F.R. §1.10 with the U.S. Postal Service on January 23, 2004, Applicants respectfully request the Patent Office correct the filing date to read —**January 23, 2004**— on all Patent Office records for this application.

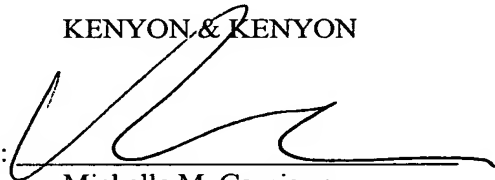
If any fees are due the Director is authorized to charge such fees to Kenyon & Kenyon's Deposit Account No. 11-0600.

Respectfully submitted,

KENYON & KENYON

Dated: 4 May 2005

By:



Michelle M. Carniaux
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One Broadway
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CUSTOMER NO. 26646



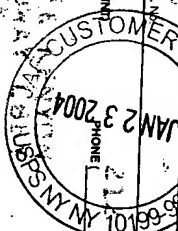
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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

**UTILITY PATENT APPLICATION
TRANSMITTAL LETTER
UNDER 37 C.F.R. 1.53(b)**

ATTORNEY DOCKET NO.:
02885/77

Address to:
Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Transmitted herewith for filing is the patent application of:

Inventor(s): **Martin VORBACH and Robert MÜNCH**

For: **METHOD OF HIERARCHICAL CACHING OF CONFIGURATION
DATA HAVING DATAFLOW PROCESSORS AND MODULES HAVING
TWO- OR MULTIDIMENSIONAL PROGRAMMABLE CELL
STRUCTURE (FPGAs, DPGAs, etc.)**

Enclosed are:

1. **63 sheets of specification, 3 sheets of claims, 1 sheet of abstract and 1 page of a translated letter to the German Patent Office in the priority application submitting 1 substitute page of claims containing corrected Claims 7 to 12.**
2. **32 sheets of drawings.**
3. **Declaration (copy from prior application (37 CFR 1.63(d)) (See 5. below).**
4. **Appointment of Power of Attorney by Assignee of Entire Interest (copy from prior application (37 CFR 1.63(d)) (See 5. below).**
5. **Incorporation by Reference. The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under 3. above is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference herein.**
6. **Applicants hereby claim Small Entity Status. See 37 C.F.R. §1.27.**
7. **Continuing application information:**

This application is a continuation of U.S. Patent Application Serial No.10/191,926, filed July 9, 2002, which is a continuation of U.S. Patent Application Serial No. 09/623,052, filed January 9, 2001.

8. An Information Disclosure Statement and Form PTO-1449 is also enclosed.
9. A Preliminary Amendment is also enclosed.
10. The filing fee has been calculated as shown below after entry of the accompanying Preliminary Amendment:

	NUMBER FILED	NUMBER EXTRA*	RATE (\$)	FEE (\$)
BASIC FEE				770.00
TOTAL CLAIMS	1 - 20 =	0	18.00	
INDEPENDENT CLAIMS	1 - 3 =	0	84.00	
MULTIPLE DEPENDENT CLAIM PRESENT			280.00	
Number extra must be zero or larger			TOTAL	770.00
If applicant is a small entity under 37 C.F.R. §§ 1.9 and 1.27, then divide total fee by 2, and enter amount here.			SMALL ENTITY TOTAL	385.00

11. Please charge the required application filing fee of **\$385.00** to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**.
12. The Commissioner is hereby authorized to charge payment of the following fees, associated with this communication or arising during the pendency of this application, or to credit any overpayment to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**:
 - A. Any additional filing fees required under 37 C.F.R. § 1.16;
 - B. Any additional patent application processing fees under 37 C.F.R. § 1.17;
 - C. Any additional patent issue fees under 37 C.F.R. § 1.18;
 - D. Any additional document supply fees under 37 C.F.R. § 1.19;
 - E. Any additional post-patent processing fees under 37 C.F.R. § 1.20; or
 - F. Any additional miscellaneous fees under 37 C.F.R. § 1.21.
13. A duplicate copy of this sheet is enclosed for charging purposes.

Dated: 23 January

By: 

Michelle M. Carniaux (Reg. No. 36,098)

KENYON & KENYON
One Broadway
New York, N.Y. 10004
Phone: (212) 425-7200



METHOD OF HIERARCHICAL CACHING OF CONFIGURATION DATA HAVING
DATAFLOW PROCESSORS AND MODULES HAVING TWO- OR
MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE
(FPGAs, DPGAs, etc.)

Background information

Related art

The related art on which this patent specification is based is
described in Patent Application 196 54 846.2-53 (Method of
automatic dynamic reloading of dataflow processors (DFPs) and
modules having a two- or multidimensional programmable cell
matrix (FPGAs, DPGAs, etc.) and in Patent Application 196 54
593. 5-53 (Run-time reconfiguration method for programmable
modules). A method of configuring and reconfiguring DFPs, as
well as FPGAs, DPGAs and similar modules according to the
related art in which a separately configured central higher-
order microcontroller-like module assumes the task of
distribution of configuration data to a plurality of lower-
order, mostly passive control units is described in these
documents.

Disadvantages of the Related Art

By using a central global unit which controls the
reconfiguration of parts (e.g. cells (CEs)) of one or more
modules, bottlenecks occur when a plurality of different
reconfiguration requests are to be handled at the same time.
The advantages of the parallelism of the above-described
modules are considerably limited by such a central unit, since
it represents the typical bottleneck and substantially slows
down the processing of data.

Furthermore, assigning the event source to the configuration
to be loaded represents a problem because absolute addresses



[2885/77]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Martin VORBACH et al.
Cont. of
Serial No. : 10/191,926
Ser. No. : To be assigned
Filed : Herewith
For : **METHOD OF HIERARCHICAL CACHING OF
CONFIGURATION DATA HAVING DATAFLOW
PROCESSORS AND MODULES HAVING TWO- OR
MULTIDIMENSIONAL PROGRAMMABLE CELL
STRUCTURE (FPGAs, DPGAs, etc.)**
Art Unit : To be assigned
Examiner : To be assigned

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

SIR:

Prior to examination, please amend the above-identified
continuation application as follows:

Amendments to the Abstract begin on page 2 of this paper.

Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of claims,
which begins on page 5 of this paper.

Remarks begin on page 6 of this paper.

Express Mail Label No.
EV 332524594US
Date of Deposit: January 23, 2004



U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

**INFORMATION DISCLOSURE
STATEMENT**

Docket Number
02885/77

Application Number
To be assigned

Filing Date
Herewith

Examiner
To be assigned

Art Unit
To be assigned

Invention Title
**METHOD OF HIERARCHICAL CACHING OF
CONFIGURATION DATA HAVING
DATAFLOW PROCESSORS AND MODULES
HAVING TWO- OR MULTIDIMENSIONAL
PROGRAMMABLE CELL STRUCTURE
(FPGAs, DPGAs, etc.)**

Inventor(s)
VORBACH et al.

Address to:
Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicants hereby bring the following references to the attention of the Examiner. The references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.
2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is not enclosed (unless otherwise noted) since they were previously cited by or submitted to the Patent Office in prior applications Serial No. 10/191,926, filed July 9, 2002, and 09/623,052, filed January 9, 2001, which are relied upon for an earlier filing date under 35 U.S.C. 120.

Dated: 23 Jan 01

By: 

Michelle M. Carniaux (Reg. No. 36,098)

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